

ABSTRACT OF THE DISCLOSURE

A PLL comprising a phase detector, a loop filter and a VCO is disclosed.

The phase detector periodically compares an externally inputted clock signal with a frequency of an internal clock signal, and outputs an output signal resulting from phase
5 difference of the two signals. The loop filter outputs a predetermined voltage in response to an output signal from said phase detector. The VCO outputs said internal clock signal having a frequency proportional to said predetermined voltage. Here, the VCO includes a capsule for adjusting the value of capacitance using an internal control signal. As a result, frequencies may be pre-compensated by control signals used in the
10 PLL. In addition, the disclosed PLL having a VCO therein can be configured into a single chip, thereby simplifying the embodiment of the whole PLL and enabling accurate compensation.